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**Risk Mitigation of Sophisticated Counterfeit ICs Using
Cost Effective Electrical Testing Techniques**

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Technical Support

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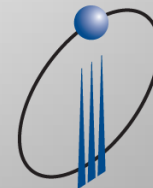
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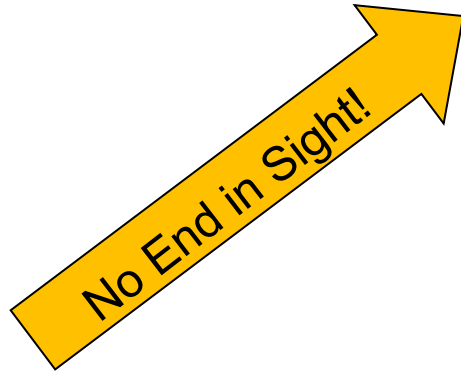
Outline

- 1. Devices keep getting more complex.**
- 2. The counterfeit problem is not going away anytime soon.**
- 3. Complex devices are being more frequently counterfeited.**
- 4. Traditional counterfeit detection techniques are no longer adequate to identify complex counterfeits.**
- 5. Full AC/DC/Functional at speed electrical test over the rated temperature is the best defense.**
- 6. What do AC, DC and Functional testing mean?**
- 7. Example complex device test development costs.**
- 8. Ways to reduce the cost complex device testing.**
- 9. Steps to follow to assure testing is performed to meet your needs.**



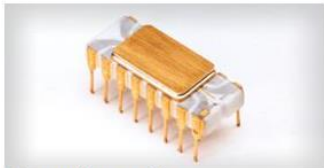
Devices keep getting more complex!

Moore's Law:
Transistor count will
double ~every 2 years.

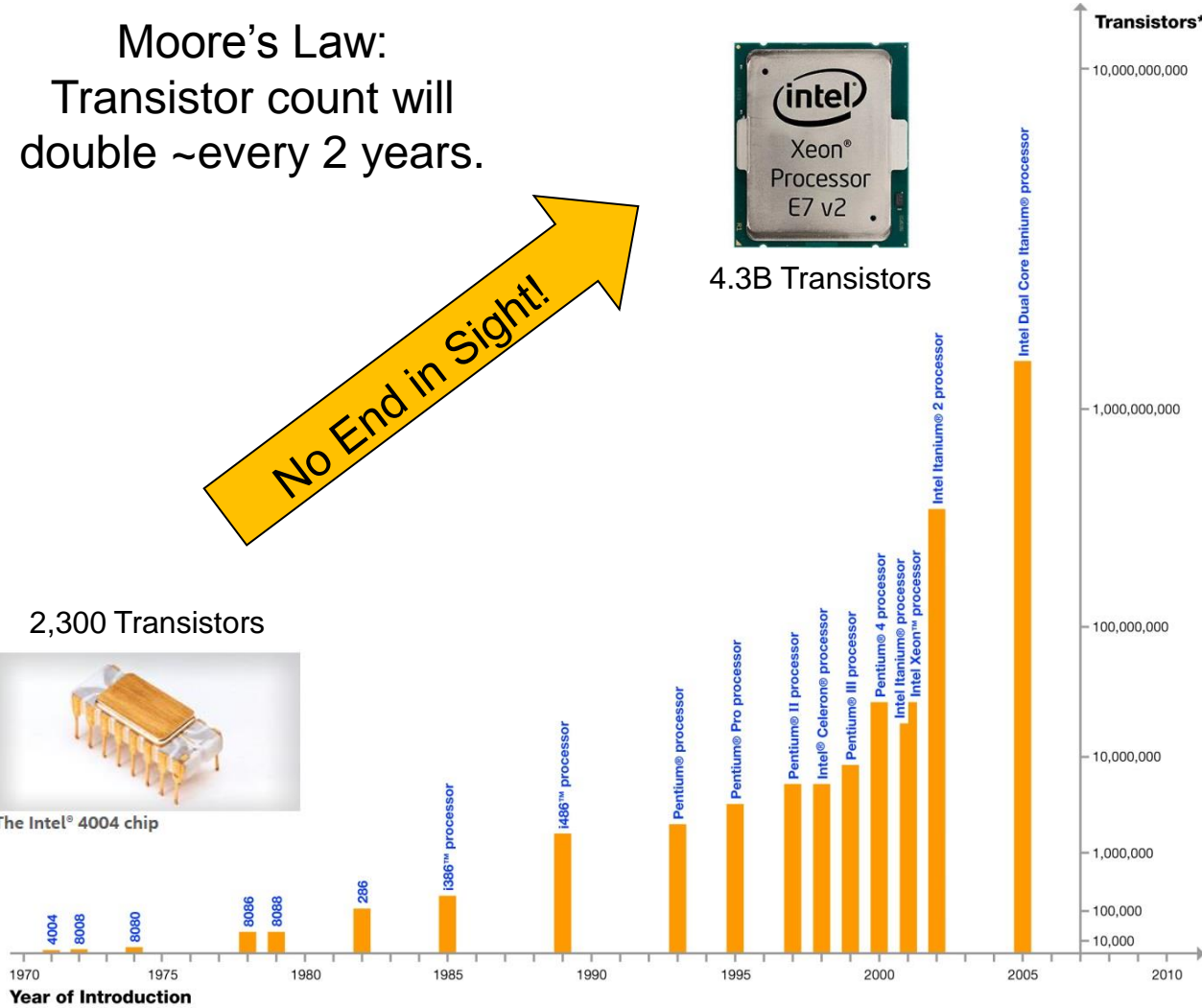


4.3B Transistors

2,300 Transistors



The Intel® 4004 chip



*Note: Vertical scale of chart not proportional to actual Transistor count.

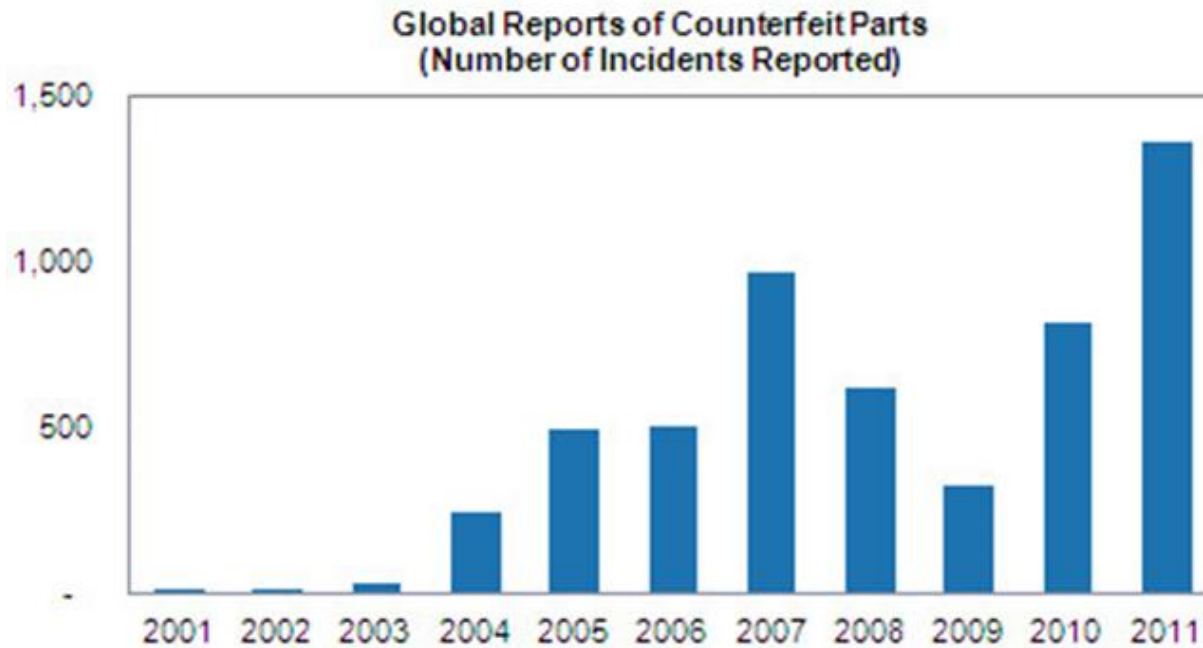
Source: Intel Corporation

Some may argue that Moore's law is beginning to slow down, but with the advent of 2.5 and 3D packaging, there is no realistic future limit to how many transistors can be in a "device."



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The Counterfeit problem continues to grow



Source: IHS Parts Management

Figures represent ERAI Suspect Counterfeit or High Risk Part Incidents and GIDEP Suspect Counterfeit Alerts for electronic components

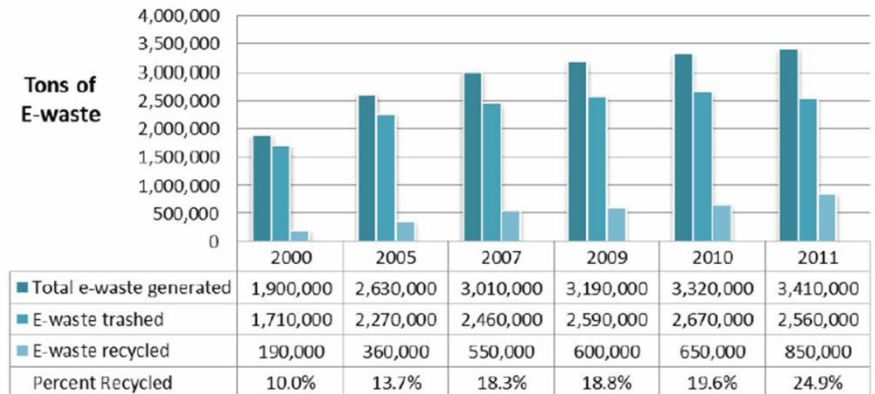


Counterfeit devices are getting more sophisticated

1. More products are being recycled creating more opportunity for reclaimed parts.
2. Newer recycled products contain more complex devices than older products.
3. Remarkable counterfeit devices are nearly indistinguishable from authentic ones.
4. Redesigned clones of simple devices are appearing – complex devices are next.



E-Waste Generation and Recycling 2000-2011



Source: electronicstakeback.com and the EPA



What can be done to eliminate counterfeit parts?

Increasing Cost/Risk



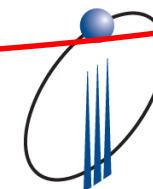
1. Buy parts from the original manufacturer or authorized distributor whenever possible (Xilinx, Avnet, Arrow).
2. Buy parts from authorized after market manufacturers (Traditionally companies like Rochester and Lansdale, but increasingly companies like Avnet and Arrow).
3. Buy parts from known sources with original paperwork traceable to the original manufacturer (another OEM that bought parts from a franchised source and has the original paperwork).
4. Do last time buys when parts become obsolete (can be expensive and hard to estimate exactly how many will be needed).
5. Qualify alternative suppliers which may not yet be obsolete (when market demand decreases usually all suppliers get out of the market).
6. Use FPGA's/ASICs to emulate obsolete devices (expensive, requires board re-layout at a minimum).
7. Redesign systems to use non-obsolete parts (most expensive option).
8. Buy parts from a reputable non-franchised broker (risk based testing and evaluation is necessary).
9. Buy parts from a questionable broker (must do full electrical test and possibly qualification).



What can be done to eliminate counterfeit parts?

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What do you do when you must buy suspect parts?

As counterfeiters become more sophisticated, full AC/DC/Functional at speed electrical testing is becoming essential.

		Detection Methods								
		External Visual & Phys Dim	XRF	X-Ray	Marking Perm Elacktop	Internal Visual	Basic DC Test	Min Func Test 25C	Full Spec Extended Temps	Test & Qual
Non Functioning Devices	No Die	Possible	No	Yes	Possible	Yes	Yes	Yes	Yes	Yes
	Wrong Die Re-Marked	Possible	No	Likely	Possible	Likely	Yes	Yes	Yes	Yes
Functioning Devices	Failed Real Parts	No	No	No	No	No	Possible	Likely	Yes	Yes
	Pulls Refurbished	Possible	Likely	No	No	No	Possible	Possible	Possible	Yes
	Speed /spec &temp up-marking	Possible	No	No	Possible	No	No	Possible	Yes	Likely
	Recovered Die	No	No	No	No	Possible	No	Possible	Possible	Likely
	Similar/ Substitution	Possible	No	No	Possible	Possible	No	Possible	Yes	Likely
	Pb Free Re-marked	Possible	Yes	No	Possible	No	No	No	No	No
	Lesser part (knock-off)	Possible	No	No	Possible	Possible	Possible	Possible	Likely	Yes

Source: Mark Marshall, Integra Technologies LLC



Standard Counterfeit Test Approaches

1. Paperwork Inspection (if any exists).
2. Gross Visual Inspection – Bent leads, package cracks, etc.
3. Fine Visual Inspection – evidence of remarking, lead contamination.
4. Remark/Resurface solvent testing
5. X-Ray – Is there a die in the package, do all the die look the same.
6. XRF – Are there any foreign elements present.
7. Decap – Die verification, size marking, etc.
8. Curve Trace – Not a true electrical test.

In the “cat and mouse” game with the counterfeiters, these mechanically oriented tests are no longer sufficient to catch complex counterfeit devices!



Standard counterfeit tests will not catch these types of counterfeits:

1. Substitution of one speed device for another.
2. Substitution of one temperature grade device for another.
3. Substitution of one die revision for another.
4. Substitution of a low power device for a high power one – & vice versa.
5. Cloned devices – redesigned exact copies of the original device.
6. Parts with ESD or electrical overstress damage not confined to the periphery of the device.
7. Original parts stolen from the manufacturer – could be passing or failing parts.
8. “Walking wounded” devices that have been mishandled in any number of ways that has caused performance degradation.

The only way to catch these types of counterfeit devices is to perform full DC, AC and Functional testing at full speed and over the full temperature range of the device.



What do the original manufacturers do?

The manufacturer must test for every conceivable application and every manufacturing defect.

The manufacturers use sophisticated simulation tools to simulate the faults and use BIST, DFT etc. in order to make sure there are no manufacturing defects and that the device performs to its datasheet limits.

This is a time consuming and expensive job.....

Fortunately for us the manufacturers have already done this testing for us on every single device - and so we as users should never see any of these failures.

Unfortunately for us, the manufacturers do not allow any after-market sources to use their proprietary test programs – so our only choice is to intelligently develop that test capability ourselves.



What can we do to eliminate complex counterfeit devices?

DC Testing - DC testing is the first step, but it actually does very little to determine if a device is counterfeit.

AC Testing - is better than DC testing alone, but still can not tell you if a device is counterfeit.

Full DC, AC and Comprehensive Functional testing at Full Speed and over the Rated Temperature Range - is the only way to gain the greatest assurance that a device is not counterfeit.

We will explore each of these in more detail.



The Example – Relatively Simple 8051 8-bit Microcontroller

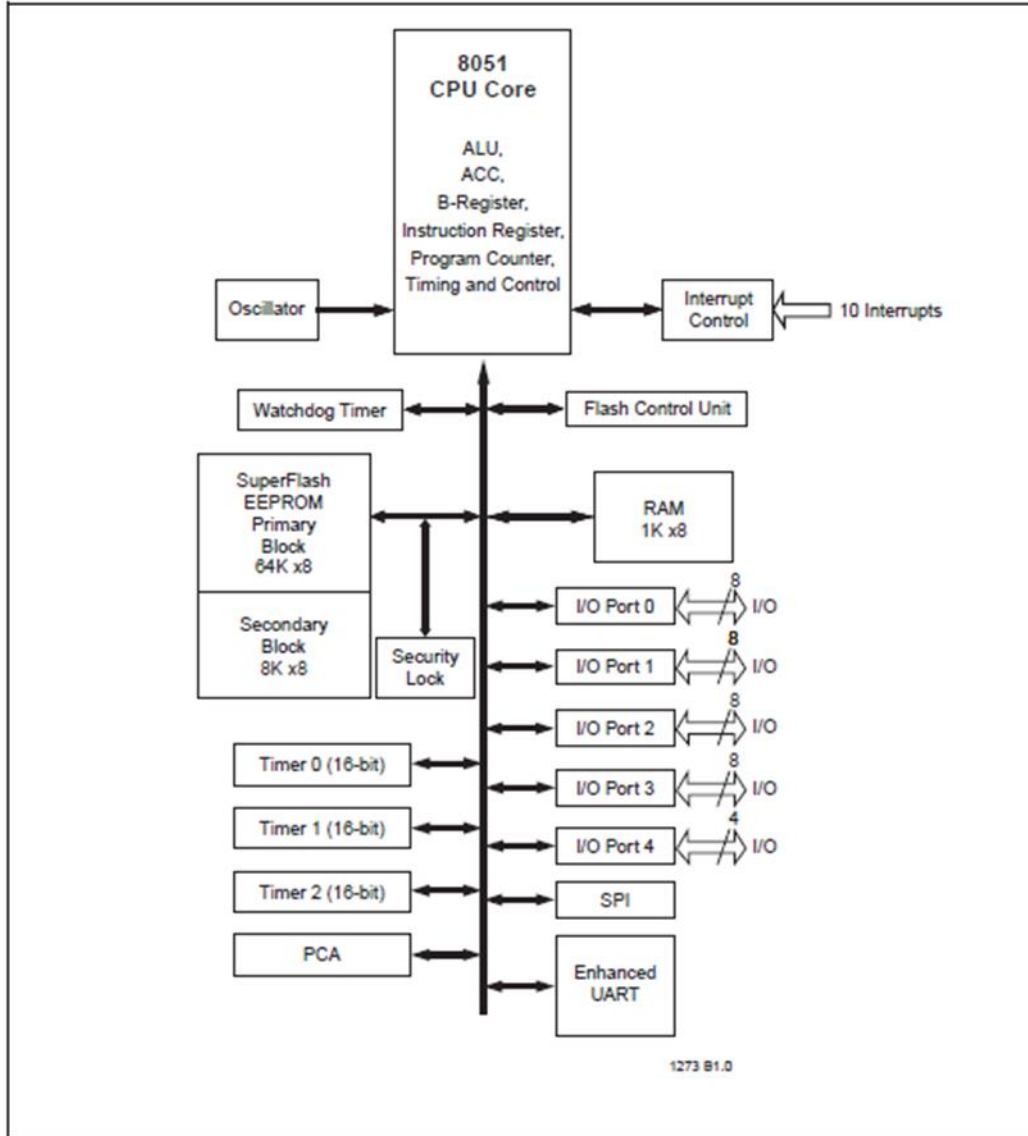
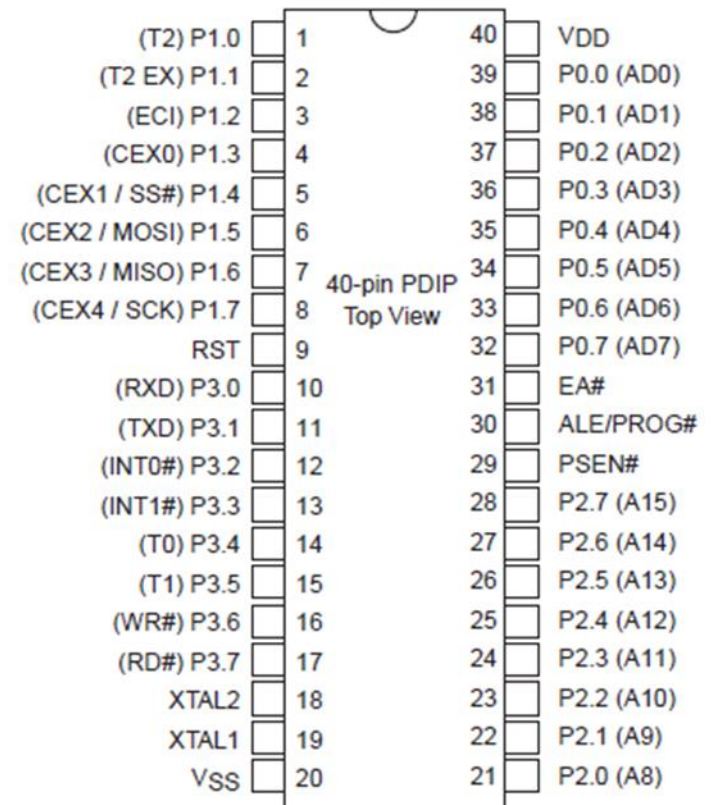


Figure 1: Functional Block Diagram

Example Block Diagram and pin-out for a legacy 8051 device.



Source: Microchip FlashFlex MCU Datasheet, 02/13

What is DC testing?

DC Electrical Characteristics

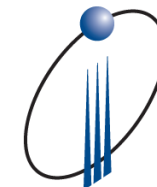
Table 36: DC Electrical Characteristics for SST89E516RDx
 $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; $V_{DD} = 4.5\text{-}5.5\text{V}$; $V_{SS} = 0\text{V}$

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Voltage	$4.5 < V_{DD} < 5.5$	-0.5	$0.2V_{DD} - 0.1$	V
V_{IH}	Input High Voltage	$4.5 < V_{DD} < 5.5$	$0.2V_{DD} + 0.9$	$V_{DD} + 0.5$	V
V_{IH1}	Input High Voltage (XTAL1, RST)	$4.5 < V_{DD} < 5.5$	$0.7V_{DD}$	$V_{DD} + 0.5$	V
V_{OL}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	$V_{DD} = 4.5\text{V}$			
		$I_{OL} = 16\text{mA}$		1.0	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3) ¹	$V_{DD} = 4.5\text{V}$			
		$I_{OL} = 100\mu\text{A}^2$		0.3	V
		$I_{OL} = 1.6\text{mA}^2$		0.45	V
		$I_{OL} = 3.5\text{mA}^2$		1.0	V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#) ^{1,3}	$V_{DD} = 4.5\text{V}$			
		$I_{OL} = 200\mu\text{A}^2$		0.3	V
		$I_{OL} = 3.2\text{mA}^2$		0.45	V
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN#) ⁴	$V_{DD} = 4.5\text{V}$			
		$I_{OH} = -10\mu\text{A}$	$V_{DD} - 0.3$		V
		$I_{OH} = -30\mu\text{A}$	$V_{DD} - 0.7$		V
		$I_{OH} = -60\mu\text{A}$	$V_{DD} - 1.5$		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode) ⁴	$V_{DD} = 4.5\text{V}$			
		$I_{OH} = -200\mu\text{A}$	$V_{DD} - 0.3$		V
		$I_{OH} = -3.2\text{mA}$	$V_{DD} - 0.7$		V
V_{BOD}	Brown-out Detection Voltage		3.85	4.15	V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	$V_{IN} = 0.4\text{V}$		-75	μA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3) ⁵	$V_{IN} = 2\text{V}$		-650	μA
I_{LI}	Input Leakage Current (Port 0)	$0.45 < V_{IN} < V_{DD} - 0.3$		± 10	μA
R_{RST}	RST Pull-down Resistor		40	225	$\text{K}\Omega$
C_{IO}	Pin Capacitance ⁶	@ 1 MHz, 25°C		15	pF
I_{DD}	Power Supply Current				
	IAP Mode @ 40 MHz			88	mA
	Active Mode @ 40 MHz			50	mA
	Idle Mode @ 40 MHz			42	mA
	Power-down Mode (min. $V_{DD} = 2\text{V}$)	$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$		80	μA
	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		90	μA	

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Example DC Parametrics Table:

This DC table looks very similar to every DC table in nearly any datasheet, regardless of the device functionality.



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Source: Microchip FlashFlex MCU Datasheet, 02/13

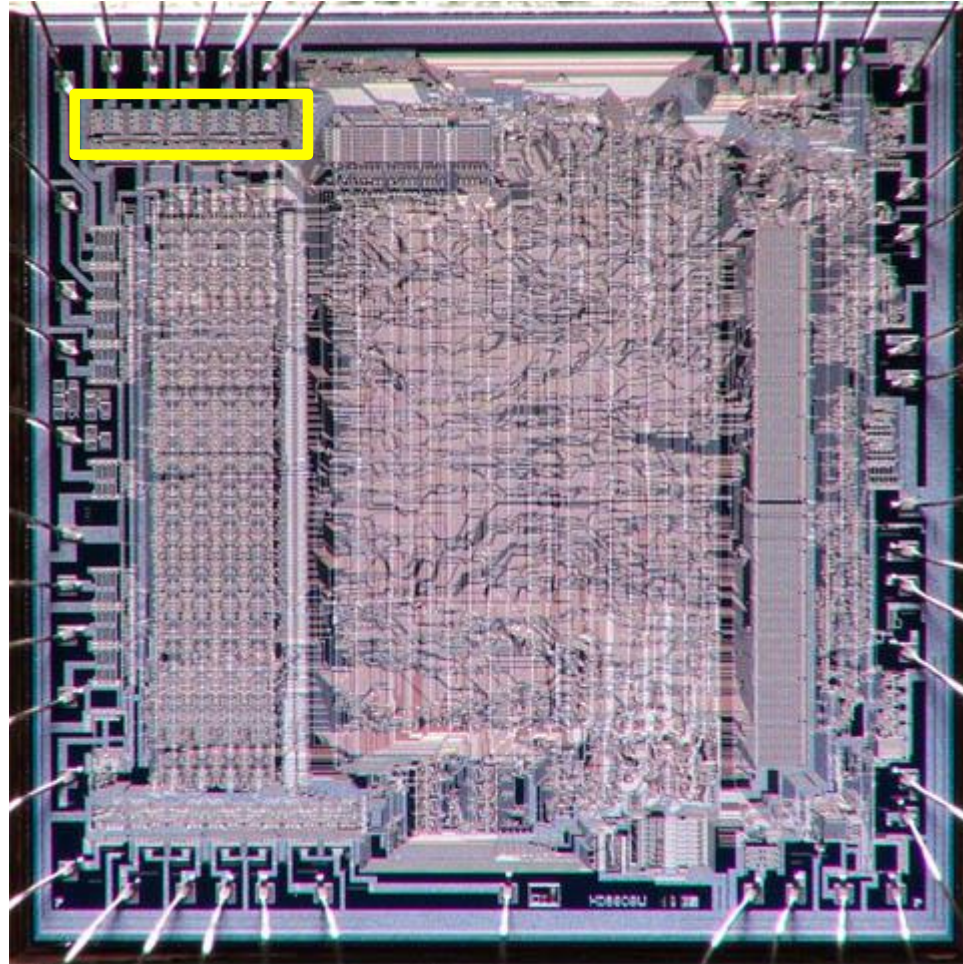
What is DC Testing?

- The DC parametrics listed in the device datasheet only represent voltage and current limits used by the device to interface it to other circuitry on a PCB.
- It also includes measuring the operating current.
- It has almost nothing to do with how the device functions.
- For instance, If you compare the DC parametrics for an Analog to Digital Converter to an a DDR3 Dynamic Ram, they look very similar, however the functionality of the devices could hardly be more different.
- DC testing only evaluates a very small percentage of the transistors along the periphery of the die.



What is DC Testing?

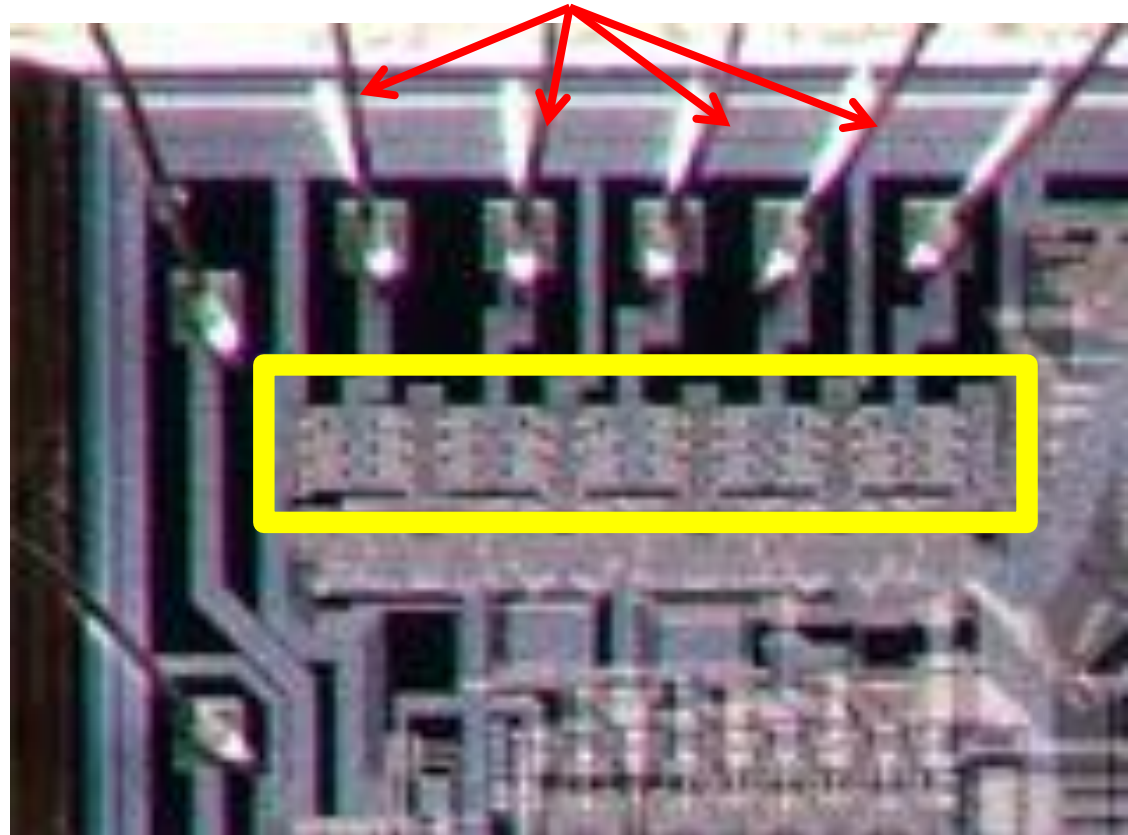
DC testing only covers the yellow circled part of the die –
Generally the first few transistors and the input diode at the entry point of the main circuitry.



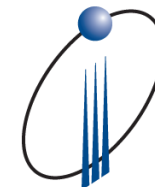
What is DC Testing?

Bond wires to the leadframe and then to the external device pins

DC testing only covers the circuitry enclosed in the yellow square - Essentially the first few transistors of each pin of the device.



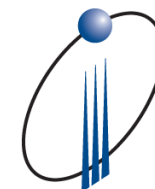
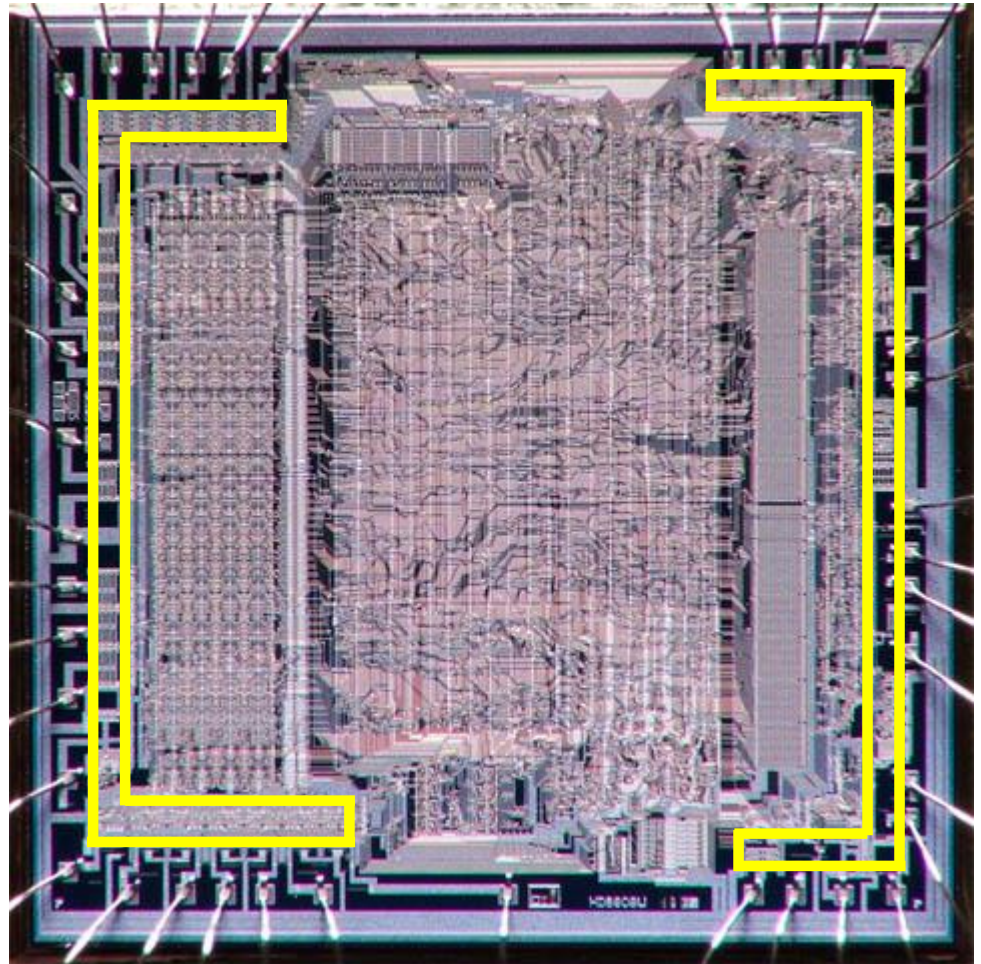
Enlarged Picture



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What is DC Testing?

The yellow portion is an estimate of the circuitry that might be tested by DC only testing - in fact it is likely a substantial overestimate of the actual circuitry being tested with DC tests.



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What can DC testing tell you?

- If an individual pin has been damaged by Electrical Over Stress (EOS) or Electro Static Discharge (ESD).
- If a pin is damaged, but not failing (indicated by higher than normal leakage current).
- IDD power supply current failures.
- Lower IDD power supply currents could indicate a low power version of the part is being substituted for a higher power version - & vice versa.



What is AC Testing?

Table 38: AC Electrical Characteristics (1 of 2)

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = 2.7\text{-}3.6\text{V}@33\text{MHz}$, $4.5\text{-}5.5\text{V}@40\text{MHz}$, $V_{SS} = 0\text{V}$

Symbol	Parameter	Oscillator						Units
		33 MHz (x1 Mode) 16 MHz (x2 Mode) ¹		40 MHz (x1 Mode) 20 MHz (x2 Mode) ¹		Variable		
		Min	Max	Min	Max	Min	Max	
$1/T_{CLCL}$	x1 Mode Oscillator Frequency	0	33	0	40	0	40	MHz
$1/2T_{CLCL}$	x2 Mode Oscillator Frequency	0	16	0	20	0	20	MHz
T_{LHLL}	ALE Pulse Width	46		35		$2T_{CLCL} - 15$		ns
T_{AVLL}	Address Valid to ALE Low	5				$T_{CLCL} - 25$ (3V)		ns
				10		$T_{CLCL} - 15$ (5V)		ns
T_{LLAX}	Address Hold After ALE Low	5				$T_{CLCL} - 25$ (3V)		ns
				10		$T_{CLCL} - 15$ (5V)		ns
T_{LLIV}	ALE Low to Valid Instr In		56				$4T_{CLCL} - 65$ (3V)	ns
					55		$4T_{CLCL} - 45$ (5V)	ns
T_{LLPL}	ALE Low to PSEN# Low	5				$T_{CLCL} - 25$ (3V)		ns
				10		$T_{CLCL} - 15$ (5V)		ns
T_{PLPH}	PSEN# Pulse Width	66		60		$3T_{CLCL} - 25$ (3V) $3T_{CLCL} - 15$ (5V)		ns
T_{PLIV}	PSEN# Low to Valid Instr In		35				$3T_{CLCL} - 55$ (3V)	ns
					25		$3T_{CLCL} - 50$ (5V)	ns
T_{PXIX}	Input Instr Hold After PSEN#					0		ns
T_{PXIZ}	Input Instr Float After PSEN#		25				$T_{CLCL} - 5$ (3V)	ns
					10		$T_{CLCL} - 15$ (5V)	ns
T_{PXAV}	PSEN# to Address valid	22		17		$T_{CLCL} - 8$		ns
T_{AVIV}	Address to Valid Instr In		72				$5T_{CLCL} - 80$ (3V)	ns
					65		$5T_{CLCL} - 60$ (5V)	ns
T_{PLAZ}	PSEN# Low to Address Float		10		10		10	ns
T_{RLRH}	RD# Pulse Width	142			120	$8T_{CLCL} - 40$ (3V) $6T_{CLCL} - 30$ (5V)		ns
T_{WLWH}	Write Pulse Width (WE#)	142			120	$8T_{CLCL} - 40$ (3V) $6T_{CLCL} - 30$ (5V)		ns
T_{RLDV}	RD# Low to Valid Data In		62				$5T_{CLCL} - 90$ (3V)	ns

Example AC Parametrics Table:

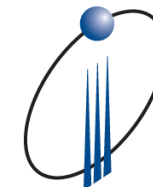
Table 38: AC Electrical Characteristics (Continued) (2 of 2)

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = 2.7\text{-}3.6\text{V}@33\text{MHz}$, $4.5\text{-}5.5\text{V}@40\text{MHz}$, $V_{SS} = 0\text{V}$

Symbol	Parameter	Oscillator						Units	
		33 MHz (x1 Mode) 16 MHz (x2 Mode) ¹		40 MHz (x1 Mode) 20 MHz (x2 Mode) ¹		Variable			
		Min	Max	Min	Max	Min	Max		
							75	$5T_{CLCL} - 50$ (5V)	ns
T_{RHDX}	Data Hold After RD#	0		0		0			ns
T_{RHDX}	Data Float After RD#		36					$2T_{CLCL} - 25$ (3V)	ns
					38			$2T_{CLCL} - 12$ (5V)	ns
T_{LLDV}	ALE Low to Valid Data In		152					$8T_{CLCL} - 90$ (3V)	ns
					150			$8T_{CLCL} - 50$ (5V)	ns
T_{AVDV}	Address to Valid Data In		183					$9T_{CLCL} - 90$ (3V)	ns
					150			$9T_{CLCL} - 75$ (5V)	ns
T_{LLWL}	ALE Low to RD# or WR# Low	66	116	60	90	$3T_{CLCL} - 25$ (3V) $3T_{CLCL} - 15$ (5V)		$3T_{CLCL} + 25$ (3V) $3T_{CLCL} + 15$ (5V)	ns
							$4T_{CLCL} - 75$ (3V)		ns
T_{AVWL}	Address to RD# or WR# Low			70				$4T_{CLCL} - 30$ (5V)	ns
								$T_{CLCL} - 27$ (3V)	ns
T_{WHQX}	Data Hold After WR#	3						$T_{CLCL} - 20$ (5V)	ns
					5			$7T_{CLCL} - 70$ (3V)	ns
T_{QVWH}	Data Valid to WR# High	142						$7T_{CLCL} - 50$ (5V)	ns
					125			$T_{CLCL} - 20$	ns
T_{QVWX}	Data Valid to WR# High to Low Transition	10		5				$T_{CLCL} - 20$	ns
T_{RLAZ}	RD# Low to Address Float		0		0			0	ns
T_{WHLH}	RD# to WR# High to ALE High	5	55			$T_{CLCL} - 25$ (3V)	$T_{CLCL} + 25$ (3V)		ns
				10	40	$T_{CLCL} - 15$ (5V)	$T_{CLCL} + 15$ (5V)		ns

1. Calculated values are for x1 Mode only

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Source: Microchip FlashFlex MCU Datasheet, 02/13

AC testing will tell you the speed at which things happen in the device like:

- How long does it take to access an address (access time).
- How long does it take for one signal occur after another (prop. delay).
- Maximum operating frequency.
- Signal rise and fall times.

But AC testing by itself, while better than just DC testing, still only tests a small percentage of the die at any one time.

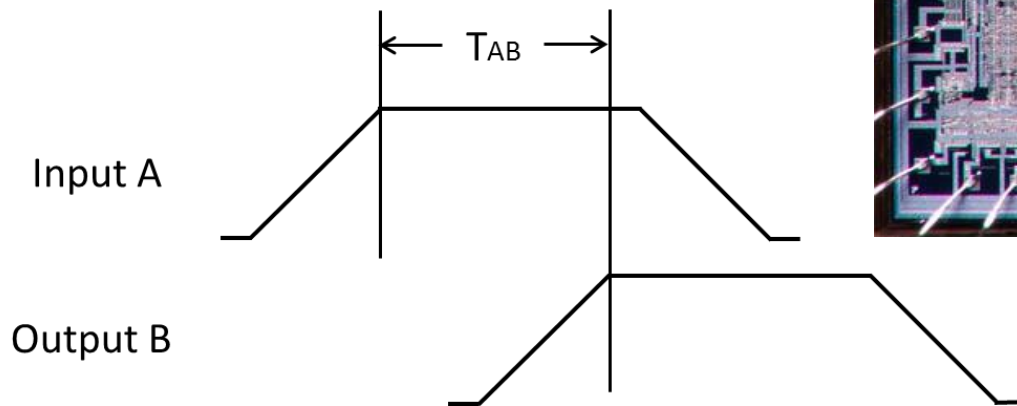
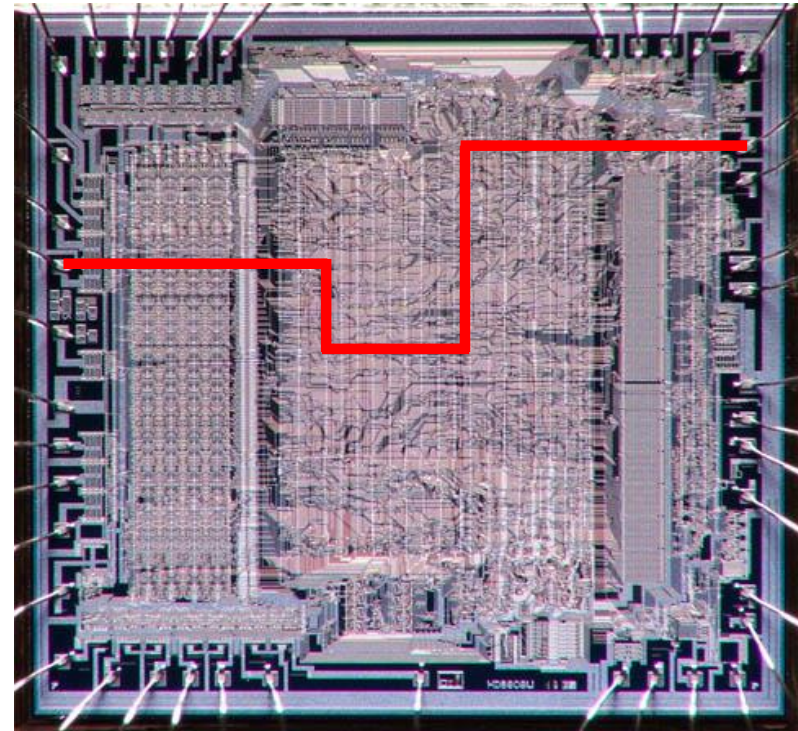


What is AC Testing?

Propagation Delay Example

Symbol	Parameter	Min	Max	Units
T_{AB}	Propagation Delay Time from Input A to Output B	5	20	ns

To measure a single AC parameter will typically only evaluate a small portion of the die – a single signal path.

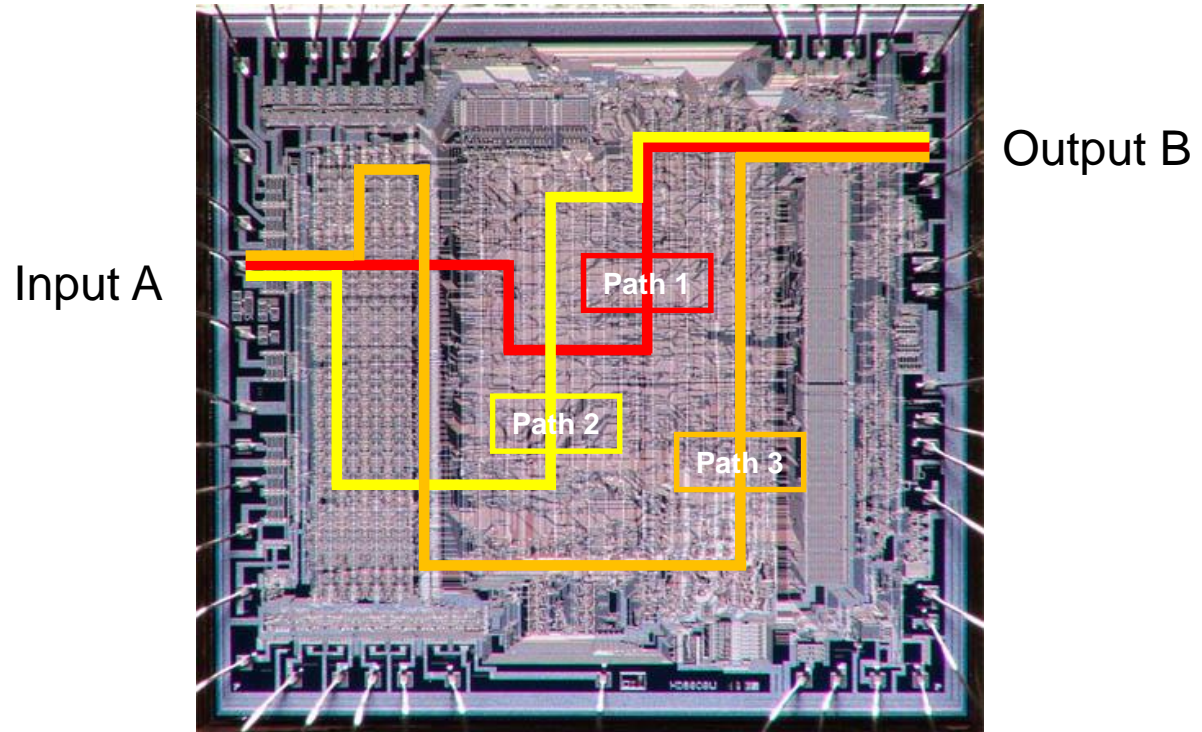


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What is AC Testing?

Propagation Delay Example

There may be several 100's or 1000's of paths through a device that are represented by a single AC parameter. The value listed in the datasheet is the worst case of all those paths. So each path needs to be evaluated to determine if they all work.



In this case there are 3 paths from Input A to Output B. Path 3 is clearly the longest and is likely the worst case propagation delay path for this AC parameter.



What is Functional Testing?

- Functional testing is making sure that all of the functions that a device can perform are exercised.
- Ironically it is usually the area of the device that is the least explained in the datasheet.
- The development of the functional test area of a complex parts accounts for 50% to 90% of the overall test development effort – and therefore the test development cost.
- Circling datasheet limits does not specify any functional tests for complex parts. It may be an adequate means of specifying tests for simple parts like Transistors and Op Amps, but it is not an adequate method for specifying testing of complex parts.

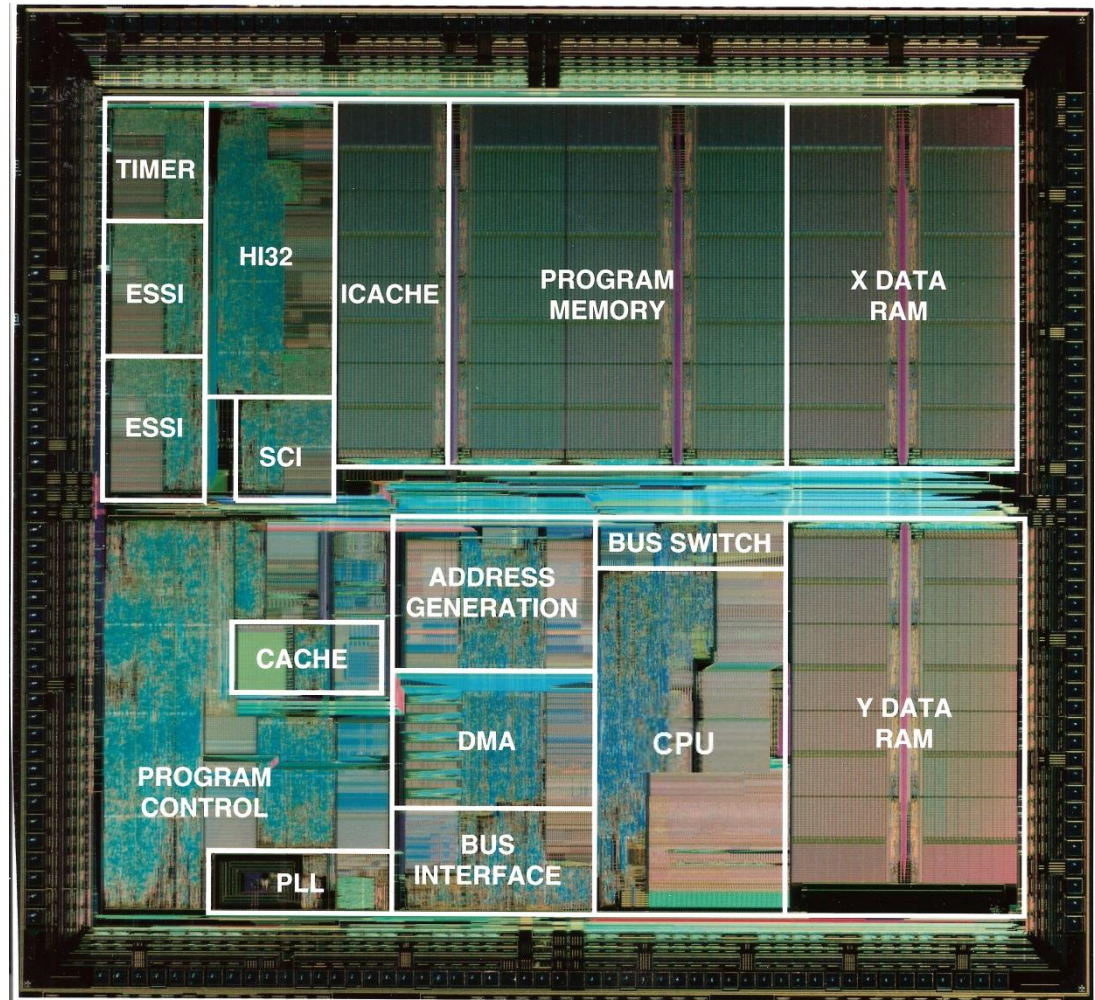


What is Functional Testing?

Functional testing requires that each functional block in a device be thoroughly tested.

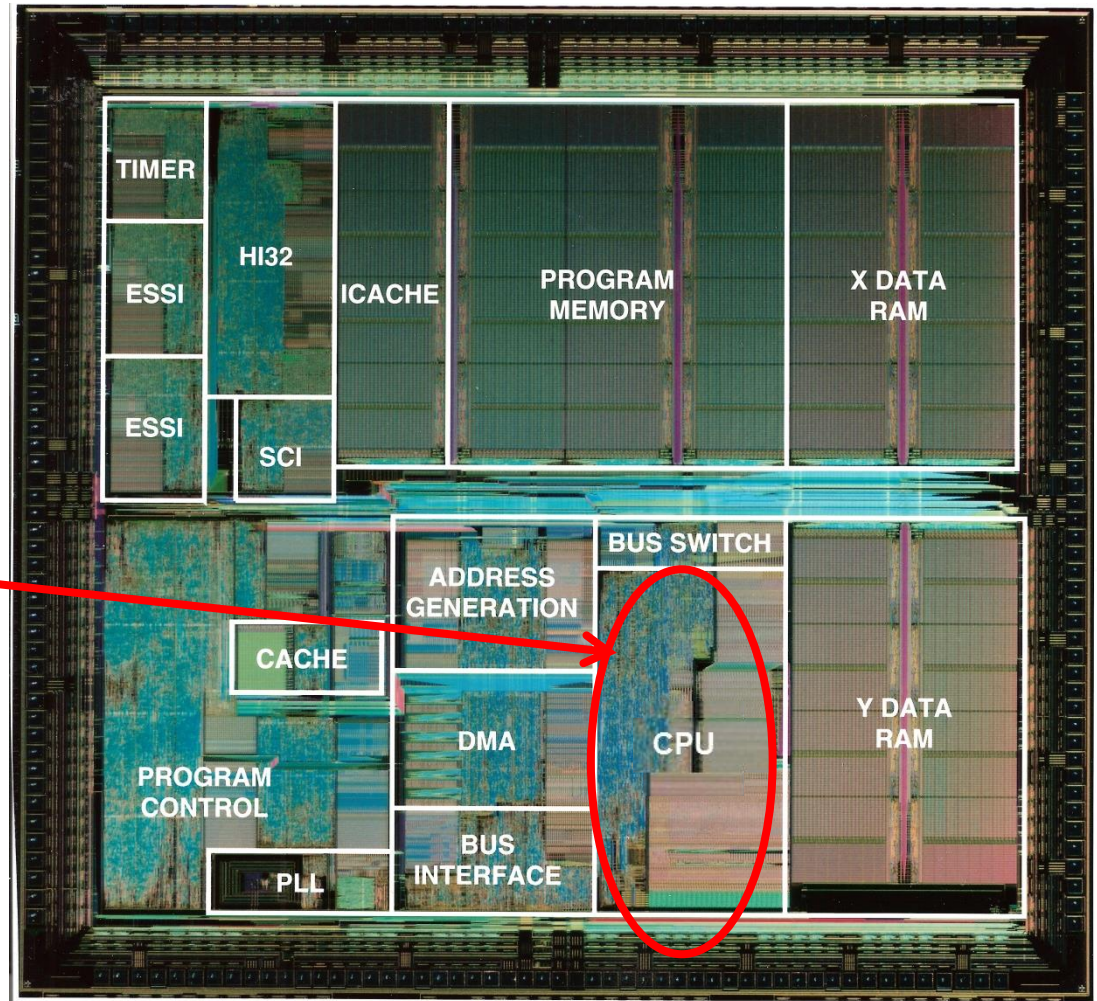
This is where up to 90% of the test development effort lies when doing a complex part.

Each white named area is a functional block for this device.



What is Functional Testing?

As an example, let's see what it might take to develop a functional test just the Central Processing Unit (CPU) on this microcontroller.



What is Functional Testing?

CPU Functional Tests

- ~112 different instructions
- 6 addressing modes
- 27 Registers
- 5 I/O Ports
- 8 bit data values = 256 possible data values
- All multiplied together

Instructions	# Types	# Data Values	# tests required to fully test
Data Transfer	29	256	7,424
Arithmetic	24	256	6,144
Logical	25	256	6,400
Bit Manipulation	12	256	3,072
Program Control	22	256	5,632
	112		28,672
Addressing Modes	6		172,032
Registers	27		4,644,864
# I/O Ports	5		23,224,320
MIM/MAX Voltage	2		46,448,640
-55C, 25C +125C	3		139,345,920

- The number of functional tests required to fully test the CPU is the result of multiplying the number of instruction types times the # of possible data values times the # addressing modes, etc.

Table Source: http://www.alciro.org/alciro/microcontroladores-8051_24/tipos-instrucciones-microcontroladores-8051_284_en.htm



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What is Functional Testing?

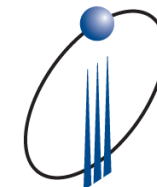
CPU Functional Tests

- ~112 different instructions
- 6 addressing modes
- 27 Registers
- 5 I/O Ports
- 8 bit data values = 256 possible data values
- All multiplied together

Instructions	# Types	# Data Values	# tests required to fully test
Data Transfer	29	256	7,424
Arithmetic	24	256	6,144
Logical	25	256	6,400
Bit Manipulation	12	256	3,072
Program Control	22	256	5,632
	112		28,672
Addressing Modes	6		172,032
Registers	27		4,644,864
# I/O Ports	5		23,224,320
MIM/MAX Voltage	2		46,448,640
-55C, 25C +125C	3		139,345,920

- The number of functional tests required to fully test the CPU is the result of multiplying the number of instruction types times the # of possible data values times the # addressing modes, etc.
- In this case that's over 23,000,000 functional tests.

Table Source: http://www.alciro.org/alciro/microcontroladores-8051_24/tipos-instrucciones-microcontroladores-8051_284_en.htm



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What is Functional Testing?

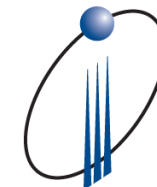
CPU Functional Tests

- ~112 different instructions
- 6 addressing modes
- 27 Registers
- 5 I/O Ports
- 8 bit data values = 256 possible data values
- All multiplied together
- Then times 2 voltages
- Then times 3 temperatures

Instructions	# Types	# Data Values	# tests required to fully test
Data Transfer	29	256	7,424
Arithmetic	24	256	6,144
Logical	25	256	6,400
Bit Manipulation	12	256	3,072
Program Control	22	256	5,632
	112		28,672
Addressing Modes	6		172,032
Registers	27		4,644,864
# I/O Ports	5		23,224,320
Min/MAX Voltage	2		46,448,640
-55C, 25C +125C	3		139,345,920

- When those 23 million functional tests are run at 2 voltages and then at 3 temperatures, the resulting number now equals **~140,000,000 functional tests!**

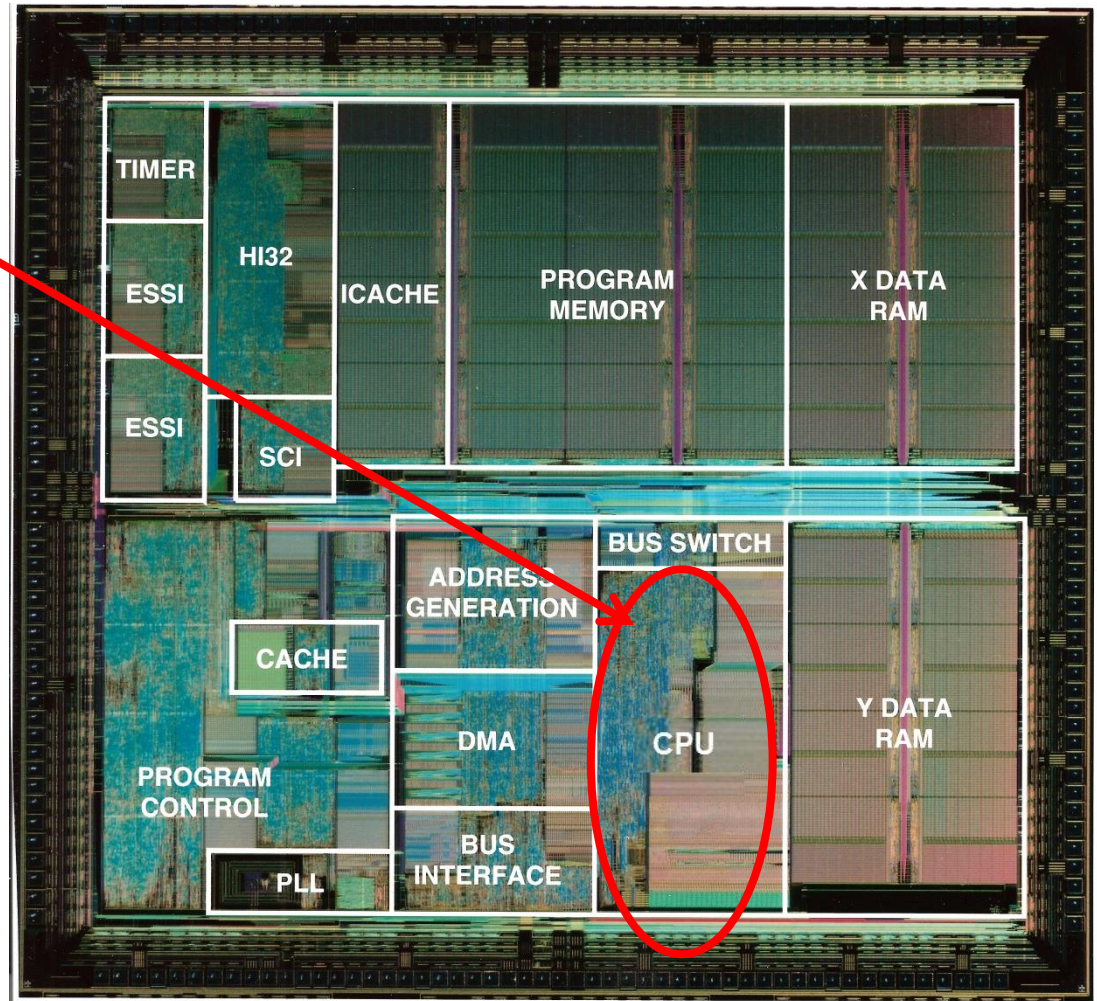
Table Source: http://www.alciro.org/alciro/microcontroladores-8051_24/tipos-instrucciones-microcontroladores-8051_284_en.htm



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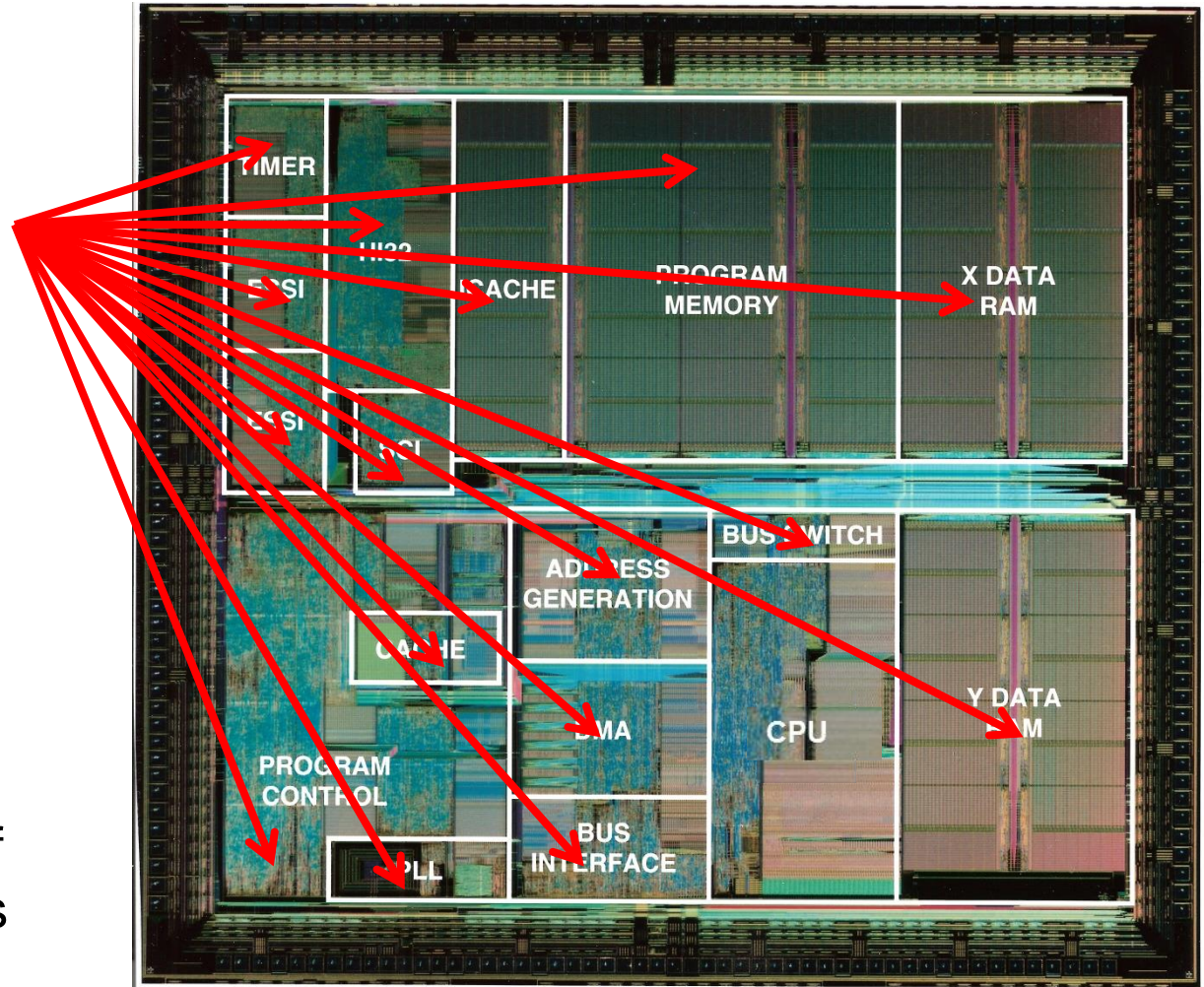
What is Functional Testing?

- And those 140 million tests just covers the CPU portion of the device.



What is Functional Testing?

- A similar approach must be taken for each of the other 16 functional blocks in this device.
- This can make functional testing very time consuming and very expensive.
- What can happen if all functional blocks are not tested?



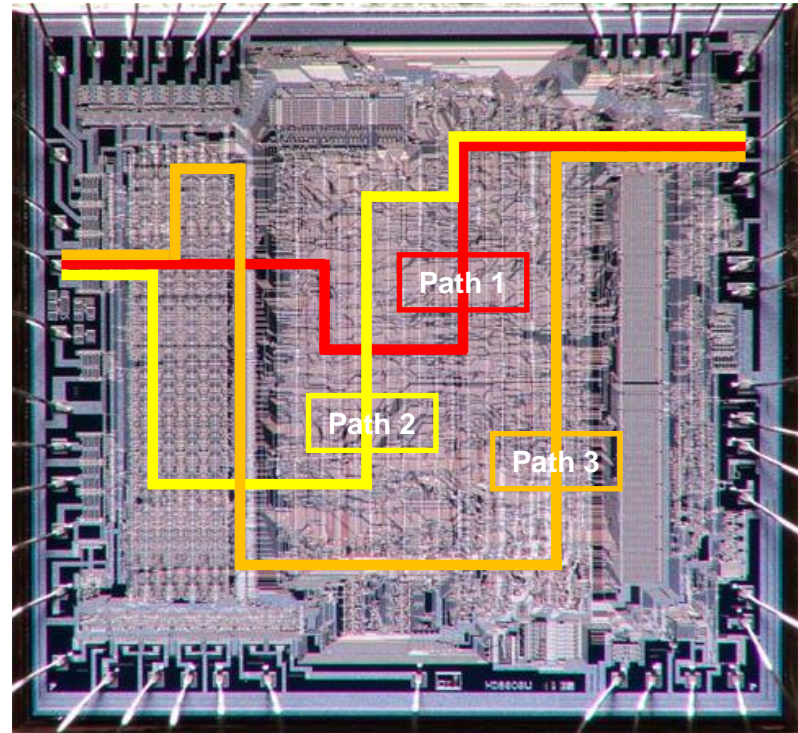
What is Functional Testing?

- What can happen if all functional blocks are not tested

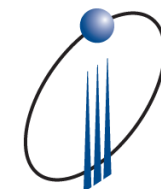
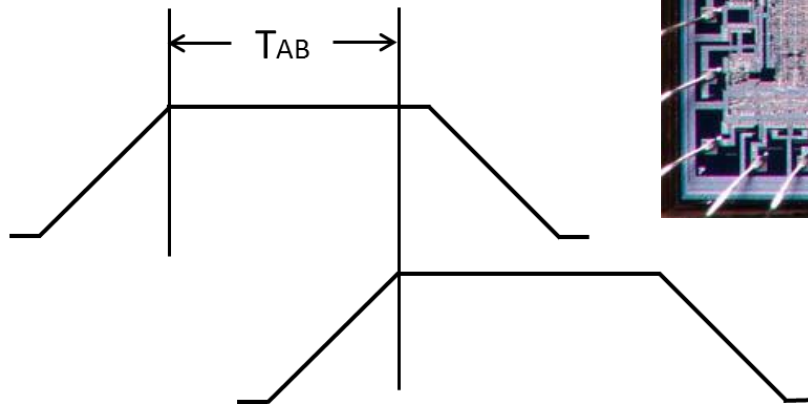
Symbol	Parameter	Min	Max	Units
T_{AB}	Propagation Delay Time from Input A to Output B	5	20	ns

- A given propagation delay can have multiple paths through different functions of the part.
- Only one path is the worst case.
- Path 3 is longer than Path 1.

Input A



Output B

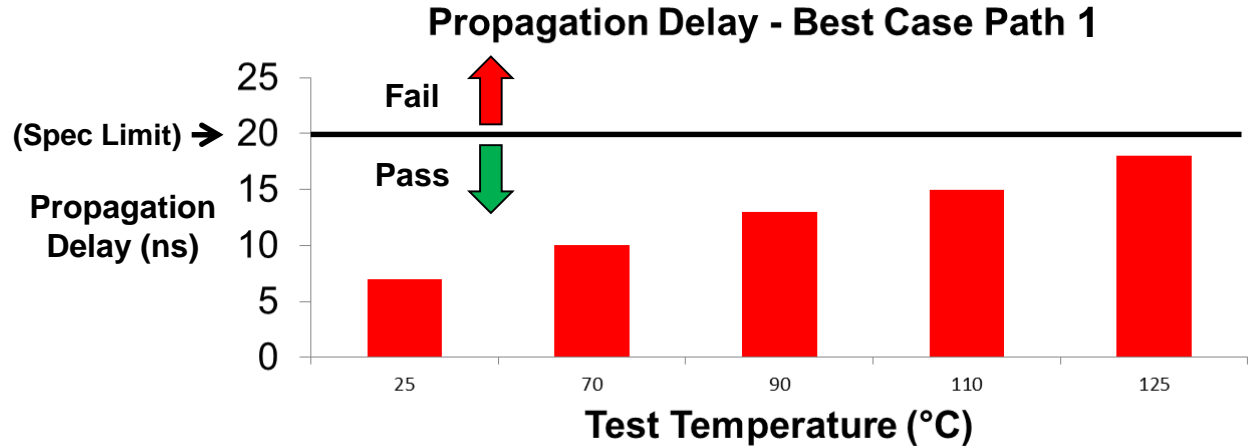


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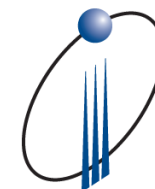
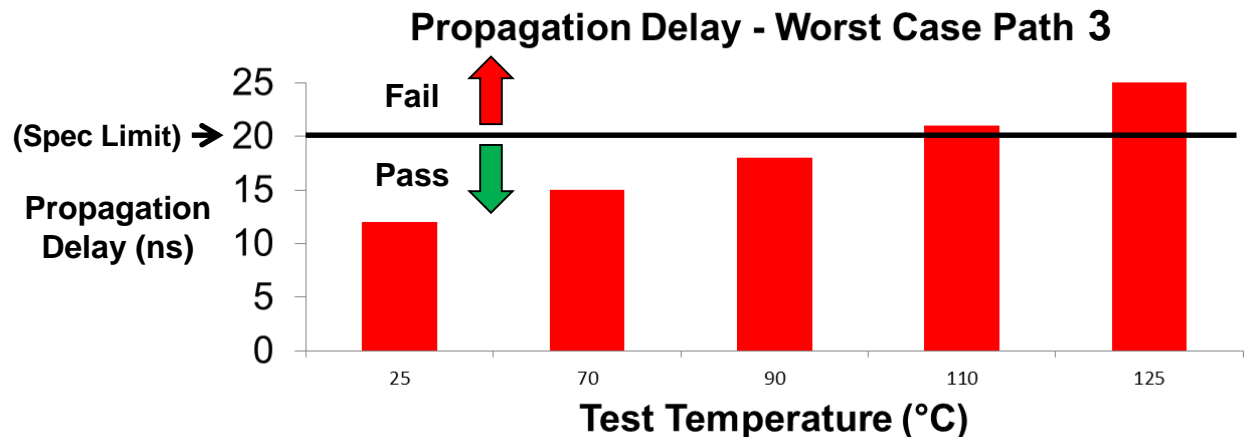
What is Functional Testing?

- What can happen if all functional blocks are not tested

Part passes its 20ns spec limit when only the best case path is tested.



Part fails its 20ns limit when the worst case path is tested.

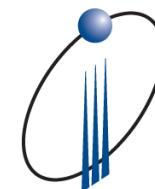
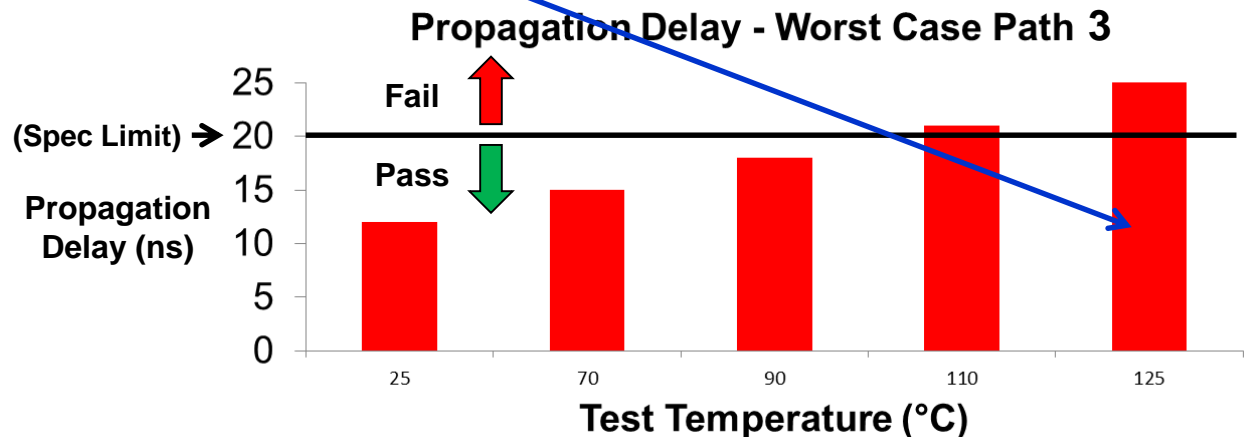
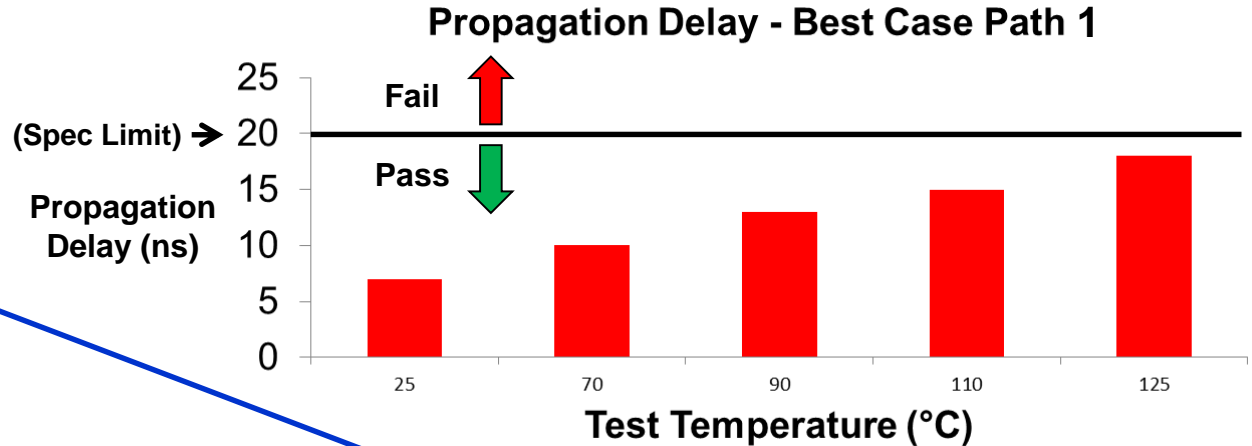


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What is Functional Testing?

- What can happen if all functional blocks are not tested

Also note that the device only fails when tested at the maximum rated temperature!



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Important Functional Testing Points:

- Functional testing is the most important part of developing a test program for complex parts.
- Yet it is often not specified in test requirements and simply left to the test lab to decide upon.
- When Functional Testing requirements are not specified, you can't be sure if your after-market purchased part will function correctly in your application.
- When Functional Testing requirements are not specified, it makes cost comparisons between test lab quotations very difficult - or even impossible.



Test Development Cost Example?

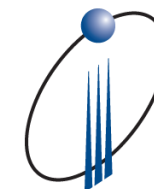
Test Development Cost Example			
Test Development Activities	Engineering Hours	Tester Hours	Cost*
Test Specification Development	20	0	\$ 3,000
Test System Selection/Speed	3	0	\$ 450
Load Board Design & Fabrication	20	5	\$ 3,750
DC Tests	25	20	\$ 6,750
Functional Test - MIN/Max Voltages	10	5	\$ 2,250
Functional Test - Timing Sets	15	10	\$ 3,750
Functional Test - CPU Core	120	80	\$ 30,000
Functional Test - Interrupt Control	30	20	\$ 7,500
Functional Test - Watchdog Timer	20	15	\$ 5,250
Functional Test - Flash Control Unit	10	7	\$ 2,550
Functional Test - SuperFlash	10	7	\$ 2,550
Functional Test - Ram	10	7	\$ 2,550
Functional Test - Security Lock	15	10	\$ 3,750
Functional Test - I/O Ports	25	17	\$ 6,300
Functional Test - Timers	25	20	\$ 6,750
Functional Test - SPI Bus	15	10	\$ 3,750
Functional Test - UART	40	30	\$ 10,500
AC Tests	60	40	\$ 15,000
Total	473	303	\$ 116,400

* Assumes \$150/hr for Engineering time and tester time

* Figures for discussion purposes only - not an actual quotation.

Comprehensive Test Program Development Quotation Example

This is how your test lab should be quoting your project.



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Test Development Cost Example?

Test Development Cost Example			
Test Development Activities	Engineering Hours	Tester Hours	Cost*
Test Specification Development	20	0	\$ 3,000
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AC Tests	60	40	\$ 15,000
Total	473	303	\$ 116,400

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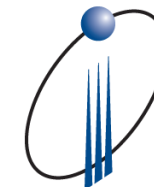
DC test requirements come from this table in the datasheet.

DC Electrical Characteristics

Table 36: DC Electrical Characteristics for SST89E516RDx
 $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; $V_{DD} = 4.5\text{-}5.5\text{V}$; $V_{SS} = 0\text{V}$

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Voltage	$4.5 < V_{DD} < 5.5$	-0.5	$0.2V_{DD} - 0.1$	V
V_{IH}	Input High Voltage	$4.5 < V_{DD} < 5.5$	$0.2V_{DD} + 0.9$	$V_{DD} + 0.5$	V
V_{IH1}	Input High Voltage (XTAL1, RST)	$4.5 < V_{DD} < 5.5$	$0.7V_{DD}$	$V_{DD} + 0.5$	V
V_{OL}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	$V_{DD} = 4.5\text{V}$ $I_{OL} = 16\text{mA}$		1.0	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3) ¹	$V_{DD} = 4.5\text{V}$ $I_{OL} = 100\mu\text{A}^2$ $I_{OL} = 1.6\text{mA}^2$ $I_{OL} = 3.6\text{mA}^2$		0.3 0.45 1.0	V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#) ^{1,3}	$V_{DD} = 4.5\text{V}$ $I_{OL} = 200\mu\text{A}^2$ $I_{OL} = 3.2\text{mA}^2$		0.3 0.45	V
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN#) ⁴	$V_{DD} = 4.5\text{V}$ $I_{OH} = -10\mu\text{A}$ $I_{OH} = -30\mu\text{A}$ $I_{OH} = -60\mu\text{A}$	$V_{DD} - 0.3$ $V_{DD} - 0.7$ $V_{DD} - 1.5$		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode) ⁴	$V_{DD} = 4.5\text{V}$ $I_{OH} = -200\mu\text{A}$ $I_{OH} = -3.2\text{mA}$	$V_{DD} - 0.3$ $V_{DD} - 0.7$		V
V_{BOD}	Brown-out Detection Voltage		3.85	4.15	V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	$V_{IN} = 0.4\text{V}$		-75	μA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3) ⁵	$V_{IN} = 2\text{V}$		-650	μA
I_{LU}	Input Leakage Current (Port 0)	$0.45 < V_{IN} < V_{DD} - 0.3$		± 10	μA
R_{RST}	RST Pull-down Resistor		40	225	$\text{K}\Omega$
C_{IO}	Pin Capacitance ⁶	@ 1 MHz, 25°C		15	pF
I_{DD}	Power Supply Current				
	IAP Mode @ 40 MHz			88	mA
	Active Mode @ 40 MHz			50	mA
	Idle Mode @ 40 MHz			42	mA
	Power-down Mode (min. $V_{DD} = 2\text{V}$)	$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		80 90	μA

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Source: Microchip FlashFlex MCU Datasheet, 02/13

Test Development Cost Example?

Test Development Cost Example			
Test Development Activities	Engineering Hours	Tester Hours	Cost*
Test Specification Development	20	0	\$ 3,000
Test System Selection/Speed	3	0	\$ 450
Load Board Design & Fabrication	20	5	\$ 3,750
DC Tests	25	20	\$ 6,750
Functional Test - MIN/Max Voltages	10	5	\$ 2,250
Functional Test - Timing Sets	15	10	\$ 3,750
Functional Test - CPU Core	120	80	\$ 30,000
Functional Test - Interrupt Control	30	20	\$ 7,500
Functional Test - Watchdog Timer	20	15	\$ 5,250
Functional Test - Flash Control Unit	10	7	\$ 2,550
Functional Test - SuperFlash	10	7	\$ 2,550
Functional Test - Ram	10	7	\$ 2,550
Functional Test - Security Lock	15	10	\$ 3,750
Functional Test - I/O Ports	25	17	\$ 6,300
Functional Test - Timers	25	20	\$ 6,750
Functional Test - SPI Bus	15	10	\$ 3,750
Functional Test - UART	40	30	\$ 10,500
AC Tests	60	40	\$ 15,000
Total	473	303	\$ 116,400

* Assumes \$150/hr for Engineering time and tester time

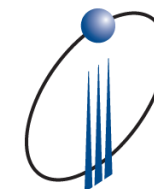
* Figures for discussion purposes only - not an actual quotation.

AC test requirements come from this table in the datasheet.

Table 38: AC Electrical Characteristics (1 of 2)

T_A = -40°C to +85°C, V_{DD} = 2.7-3.6V@33MHz, 4.5-5.5V@40MHz, V_{SS} = 0V

Symbol	Parameter	Oscillator						Units
		33 MHz (x1 Mode) 16 MHz (x2 Mode) ¹		40 MHz (x1 Mode) 20 MHz (x2 Mode) ¹		Variable		
		Min	Max	Min	Max	Min	Max	
1/T _{CLCL}	x1 Mode Oscillator Frequency	0	33	0	40	0	40	MHz
1/2T _{CLCL}	x2 Mode Oscillator Frequency	0	16	0	20	0	20	MHz
T _{LHLL}	ALE Pulse Width	48		35		2T _{CLCL} - 15		ns
T _{AVLL}	Address Valid to ALE Low	5				T _{CLCL} - 25 (3V)		ns
				10		T _{CLCL} - 15 (5V)		ns
T _{LLEX}	Address Hold After ALE Low	5				T _{CLCL} - 25 (3V)		ns
				10		T _{CLCL} - 15 (5V)		ns
T _{LLEV}	ALE Low to Valid Instr In		56				4T _{CLCL} - 65 (3V)	ns
					55		4T _{CLCL} - 45 (5V)	ns
T _{LLEL}	ALE Low to PSEN# Low	5				T _{CLCL} - 25 (3V)		ns
				10		T _{CLCL} - 15 (5V)		ns
T _{PLPH}	PSEN# Pulse Width	66		60		3T _{CLCL} - 25 (3V)		ns
						3T _{CLCL} - 15 (5V)		ns
T _{PLIV}	PSEN# Low to Valid Instr In		35				3T _{CLCL} - 55 (3V)	ns
					25		3T _{CLCL} - 50 (5V)	ns
T _{PIX}	Input Instr Hold After PSEN#					0		ns
T _{PIXZ}	Input Instr Float After PSEN#		25				T _{CLCL} - 5 (3V)	ns
					10		T _{CLCL} - 15 (5V)	ns
T _{PIXV}	PSEN# to Address valid	22		17		T _{CLCL} - 8		ns
T _{AVIV}	Address to Valid Instr In		72				5T _{CLCL} - 80 (3V)	ns
					65		5T _{CLCL} - 60 (5V)	ns
T _{PLAZ}	PSEN# Low to Address Float		10		10		10	ns
T _{RLRH}	RD# Pulse Width	142		120		6T _{CLCL} - 40 (3V)		ns
						6T _{CLCL} - 30 (5V)		ns
T _{WLWH}	Write Pulse Width (WE#)	142		120		6T _{CLCL} - 40 (3V)		ns
						6T _{CLCL} - 30 (5V)		ns
T _{RLDV}	RD# Low to Valid Data In		62				5T _{CLCL} - 90 (3V)	ns



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Source: Microchip FlashFlex MCU Datasheet, 02/13

Test Development Cost Example?

Test Development Cost Example			
Test Development Activities	Engineering Hours	Tester Hours	Cost*
Test Specification Development	20	0	\$ 3,000
Test System Selection/Speed	3	0	\$ 450
Load Board Design & Fabrication	20	5	\$ 3,750
DC Tests	25	20	\$ 6,750
Functional Test - MIN/Max Voltages	10	5	\$ 2,250
Functional Test - Timing Sets	15	10	\$ 3,750
Functional Test - CPU Core	120	80	\$ 30,000
Functional Test - Interrupt Control	30	20	\$ 7,500
Functional Test - Watchdog Timer	20	15	\$ 5,250
Functional Test - Flash Control Unit	10	7	\$ 2,550
Functional Test - SuperFlash	10	7	\$ 2,550
Functional Test - Ram	10	7	\$ 2,550
Functional Test - Security Lock	15	10	\$ 3,750
Functional Test - I/O Ports	25	17	\$ 6,300
Functional Test - Timers	25	20	\$ 6,750
Functional Test - SPI Bus	15	10	\$ 3,750
Functional Test - UART	40	30	\$ 10,500
AC Tests	60	40	\$ 15,000
Total	473	303	\$ 116,400

* Assumes \$150/hr for Engineering time and tester time

* Figures for discussion purposes only - not an actual quotation.

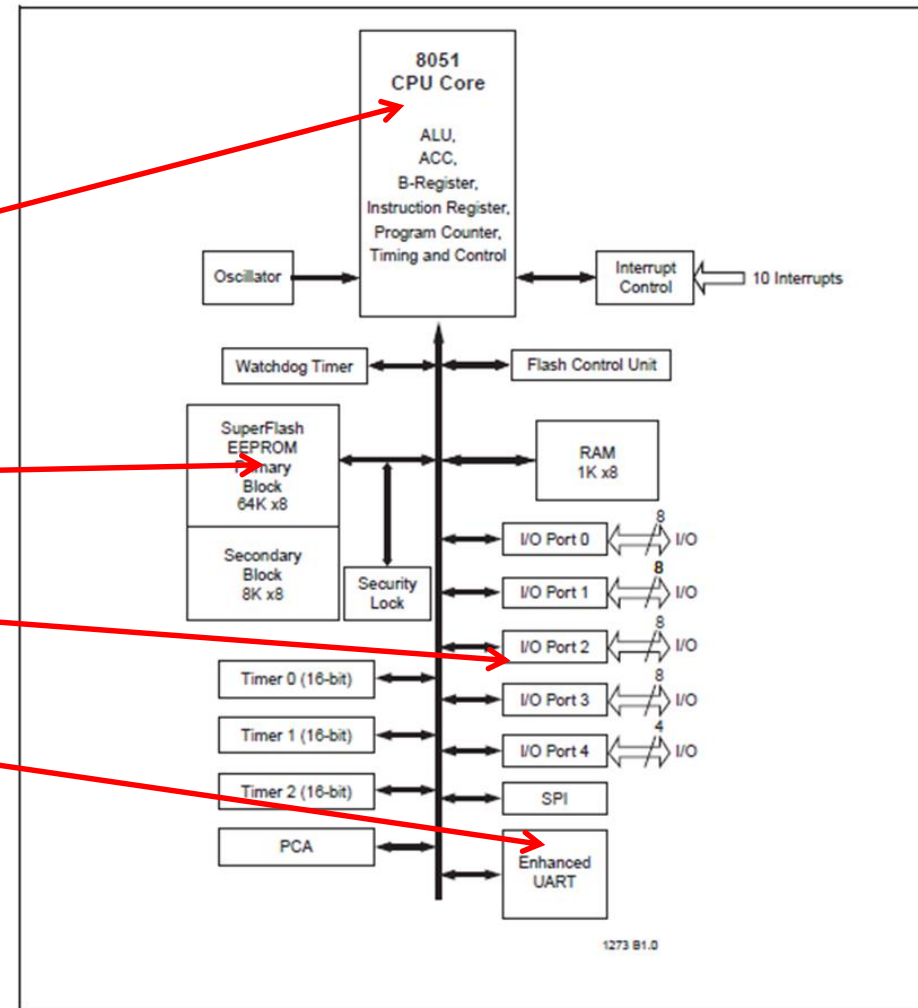
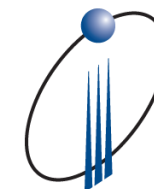


Figure 1: Functional Block Diagram

Functional test requirements come from this block diagram in the datasheet and a separate programming guide.



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Source: Microchip FlashFlex MCU Datasheet, 02/13

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Total	473	303	\$ 116,400

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* Figures for discussion purposes only - not an actual quotation.

Test Development Percentage Effort			
Test Development Activities	Engineering Hours	Tester Hours	% Effort
Misc Test Development Items	43	5	9%
DC Tests	25	20	5%
Functional Tests	345	238	73%
AC Tests	60	40	13%
Total	473	303	100%

73% of effort/cost is in functional test development

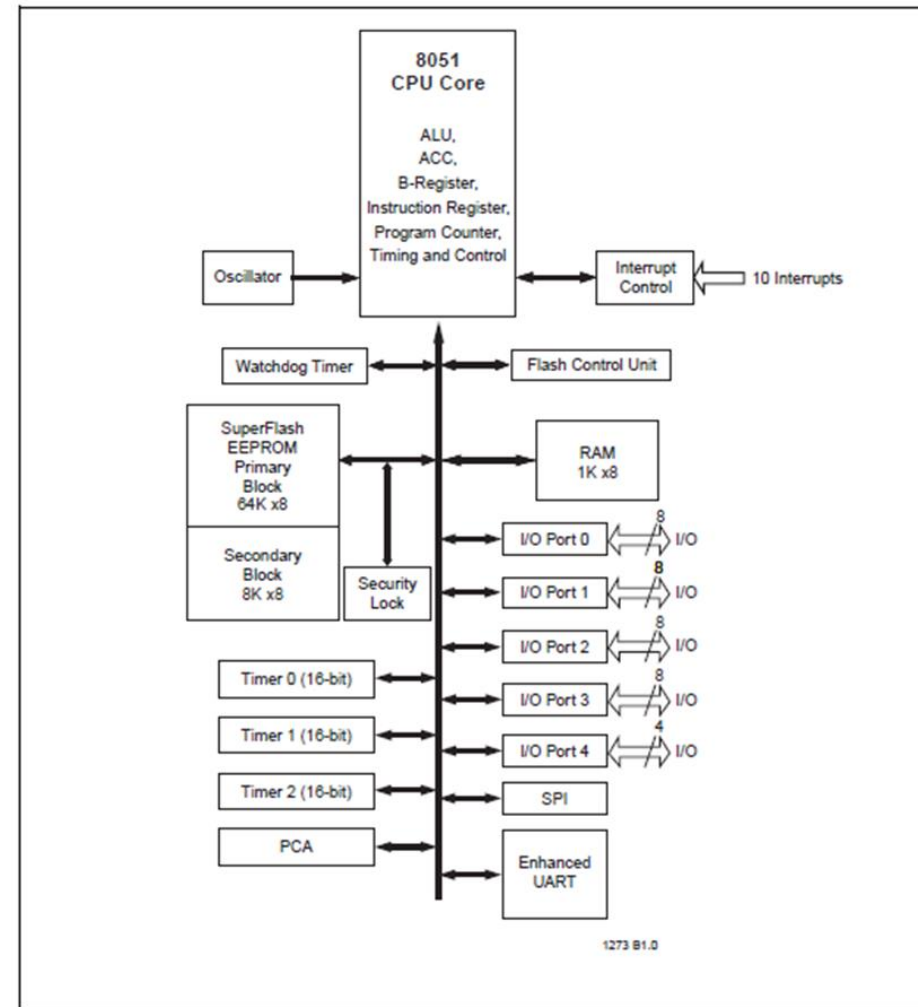


Figure 1: Functional Block Diagram

Source: Microchip FlashFlex MCU Datasheet, 02/13



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The Test Specification is critical

- Clearly defining exactly what tests need to be done and under what conditions will assure that an adequate test is performed.
- The test specification can also help reduce costs by not testing functions that are not important to the application – this will be discussed more later.

- Spend the time to be clear up front about what tests need to be run and under what conditions – this will assure you get the test you need.



Test Development Cost Example?

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Total	473	303	\$ 116,400

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* Figures for discussion purposes only - not an actual quotation.

Test System selection is critical

- Test system must be capable of testing at full device speed.
- If you have a 500MHz max operating frequency device, the tester **MUST** be also be capable of testing at 500MHz.
- The hourly rate of the tester is proportional to its performance, so choose the test system that has the lowest performance that can meet the device's performance requirements.

- Don't settle for a tester with lower performance than your device requires.
- Don't pay for a tester with more performance than you need.
- Be sure the engineer writing the test program has sufficient experience.



Saving Test Development Costs

Since the manufacturer has already thoroughly tested the devices as a part of their original manufacturing flow, the developer is able to limit the counterfeit device testing to match only the actual application conditions.

1. Use actual application speeds.
2. Use actual application programming code (uP and memory).
3. Use actual application designs (FPGA).
4. Test only functional blocks actually used in the application.
5. Test only the AC parameters that are critical to the application.
6. Leverage test programs already developed for the same or similar parts.
7. Use device emulators.
8. Use golden devices to “learn” device functionality.

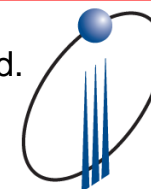


How can test development costs be saved?

Test Development Cost Example				Cost Savings Opportunities			
Test Development Activities	Engineering Hours	Tester Hours	Cost	Description	Engineering Hours	Tester Hours	Cost
Test Specification Development	20	0	\$ 3,000	Don't cut back here	20	0	\$ 3,000
Test System Selection/Speed	3	0	\$ 450	Don't cut back here	3	0	\$ 450
Load Board Design & Fabrication	20	5	\$ 3,750	Don't cut back here	20	5	\$ 3,500
DC Tests	25	20	\$ 6,750	Don't cut back here	25	20	\$ 5,750
Functional Test - MIN/Max Voltages	10	5	\$ 2,250	Don't cut back here	10	5	\$ 2,000
Functional Test - Timing Sets	15	10	\$ 3,750	Test only application timing	5	7	\$ 1,450
Functional Test - CPU Core	120	80	\$ 30,000	Use actual code from application	40	30	\$ 9,000
Functional Test - Interrupt Control	30	20	\$ 7,500	Only 1 interrupt used in application	10	7	\$ 2,200
Functional Test - Watchdog Timer	20	15	\$ 5,250	Assume full test needed - No Change	20	15	\$ 4,500
Functional Test - Flash Control Unit	10	7	\$ 2,550	Assume full test needed - No Change	10	7	\$ 2,200
Functional Test - SuperFlash	10	7	\$ 2,550	Assume full test needed - No Change	10	7	\$ 2,200
Functional Test - Ram	10	7	\$ 2,550	Assume full test needed - No Change	10	7	\$ 2,200
Functional Test - Security Lock	15	10	\$ 3,750	Not used in application	0	0	\$ -
Functional Test - I/O Ports	25	17	\$ 6,300	Assume only one I/O Port used	5	3	\$ 1,050
Functional Test - Timers	25	20	\$ 6,750	Not used in application	0	0	\$ -
Functional Test - SPI Bus	15	10	\$ 3,750	Not used in application	0	0	\$ -
Functional Test - UART	40	30	\$ 10,500	Not used in application	0	0	\$ -
AC Tests	60	40	\$ 15,000	Only 1/3 of AC's important for application	20	15	\$ 4,500
Total	473	303	\$ 116,400	Total	208	128	\$ 44,000

A test savings of \$72,400 (62%) was achieved by matching the test program performance to the actual device application!!

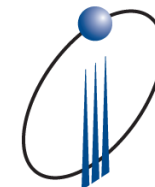
- Tester rate lowered from \$150/hr to \$100/hr by testing at actual application speed.
- Functional and AC tests matched only the actual end application needs.
- Engineering rate assumed to remain the same – a good engineer is still needed.



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Steps to follow to assure you receive the testing you need:

1. Fully understand you device application.
2. Develop a comprehensive test specification that reflects your application needs.
3. Choose a test lab that has the equipment and engineering capability to **fully** test to your test specification, but not over test.
4. Demand a detailed response from your test lab that shows the equipment to be used and its configuration. Make sure the equipment meets your requirements.
5. Read all notes included in quotations received from your test lab. Test exceptions, if any, should be clearly noted, but are sometimes hard to find.
6. When comparing test lab price quotations, be sure both labs are quoting the same AC, DC, Functional and Full Speed test coverage over the specified temperature range. If one test labs price looks significantly lower than the other – it probably means they are quoting less test coverage.
7. Perform an on site detailed test review of all test conditions and limits prior to releasing the test program for production. Unscrupulous test labs sometimes arbitrarily change or eliminate difficult tests they can't get to work.
8. Provide examples of failing devices if you have them and be sure the test program can catch them.



Summary

- 1. Devices keep getting more complex.**
- 2. The counterfeit problem is not going away anytime soon.**
- 3. Complex devices are being more frequently counterfeited.**
- 4. Traditional counterfeit detection techniques are no longer adequate to identify complex counterfeits.**
- 5. Full AC/DC/Functional at speed electrical test over the rated temperature is the best defense.**
- 6. There are effective ways to cost effectively test complex devices.**
- 7. Spend the time to develop a test specification that meets your application needs and cost targets.**
- 8. Select a test lab that has the equipment and engineering capability to fully test your device.**
- 9. When evaluating test lab proposals, be sure both labs are making the same assumptions about meeting your test specification – there are often many differences.**



Thank you from the Employee Owners of Integra Technologies!!



Integra Technologies LLC, along with the recently acquired Analytical Solutions, has been providing one of the broadest ranges of test and evaluation services in our industry for over 30 years. Our services include:

Test Development

Final Test

Characterization

Wafer Probe

Upscreening

Failure Analysis

Counterfeit Detection

PEM Qualifications

Qualification Services (HTOL, HAST, Temp Cycle, etc.)

Assembly/Repackaging (outsourced to qualified partners)

MIL-STD 883 and 750 Testing

Volume Production Test

Destructive Physical Analysis

Obsolescence Management

We are approved by DLA for MIL-STD-883 & 750 processing, ITAR, ISO 9001, AS9100 and DMEA Category 1 "Trusted"

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